Listing and Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1.(currently amended) Method for communication between an IC and an external DRAM, where the external DRAM has at least one memory bank and communicates with the IC via two or more channels, wherein the transmission of memory bank commands of multiple channels is prioritized on the basis of a static priority allocation for commands and a dynamic priority allocation for the channels.

2.(previously presented) Method according to Claim 1, wherein the static priority allocation for commands involves a 'Burst Terminate' command being given the highest, a 'Read' or 'Write' command being given the second highest, an 'Activate' command being given the third highest and a 'Precharge' command being given the lowest priority.

3.(currently amended) Method according to Claim 1, wherein the dynamic priority allocation for channels involves a channel being given the lowest priority after [[an]] a command has been sent.

4.(previously presented) Method according to Claim 1, wherein the dynamic priority allocation involves one of the channels being given the highest priority in the next clock cycle if it does not have the highest priority in the current clock cycle and another channel sends a command.

5.(currently amended) Method according to Claim 1, wherein the dynamic priority allocation ~~may involve~~ involves one of the channels losing the highest priority only when it can send a command.

6.(previously presented) Method according to Claim 1, wherein the channels access physically separate memory areas in the external DRAM.

7.(previously presented) Method according to Claim 1, wherein the channels access jointly used memory areas in the external DRAM and the assurance is given that no successive access operations to a jointly used memory area will arise.

8.(previously presented) Method according to Claim 1, wherein a network is provided which allows at least one channel to access various memory banks.

9.(previously presented) Method according to Claim 1, wherein two access operations to a memory bank always have an access operation to another memory bank effected between them.

10.(previously presented) Method according to Claim 1, wherein two successive access operations to a memory bank are permitted when they are made to the same row in the memory bank.

11.(previously presented) Method according to Claim 1, wherein the states of the memory banks are depicted by associated state machines.

12.(currently amended) Method according to Claim 1, wherein a plurality of DRAM modules are used and a chip enable signal is transmitted in order to select the desired module.

13.(currently amended) Memory controller for an IC with an external DRAM, where the external DRAM has at least one memory bank and communicates with the IC via two or more channels, wherein it has a command scheduler which prioritizes the transmission of memory bank commands of multiple channels on the basis of a static priority allocation for commands and a dynamic priority allocation for the channels.

14.(currently amended) Appliance for reading and/or writing to storage media, wherein [[it]] the appliance comprising a memory controller utilizing the ~~uses a~~ method according to Claim 1 ~~or has a memory controller~~.